38-GHz-Band High-Power MMIC Amplifier Module For Satellites On-Board Use

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Abstract—**This paper presents the design and development results of 38-GHz high-power MMIC amplifier modules for use in the solid state power amplifier (SSPA) to be carried aboard Engineering Test Satellite VI in 1993. This amplifier will be used in millimeter-wave inter-satellite communication experiments. For the development of this amplifier, we designed high-power, highly reliable FET's with 0.25 μm-long gates. The FET large-signal impedance was accurately measured using an improved load-pull method and MMIC transformers. The measurements were used to design two types of MMIC's: one composed of two FET cells with 600 μm wide gates, and the other of four FET cells with 400 μm wide gates. We also developed a two-stage amplifier package consisting of two of these MMIC's that can be used at 38 GHz. We obtained a Po (1 dB) of 25 dBm and a gain of 11 dB. A 38-GHz test conducted during chip screening achieves a high production yield without circuits adjustment.**

I. Introduction

SINCE the first artificial satellite was launched in 1957, the launch of numerous communications, broadcast and observation satellites quickly followed. The increased traffic of communication has stimulated research and development of new satellite communications systems. Techniques under consideration include frequency reuse, land mobile satellite communications, and inter-satellite communications. In Japan millimeter-wave satellite communications experiments [1] are being planned under the aegis of the Ministry of Posts and Telecommunications Communications. These experiments will involve Engineering Test Satellite VI (ETS-VI), due for launch in 1993.

Technological improvement has steadily increased the power output and operating frequency of the solid-states power amplifiers (SSPA's) [2]–[6]. Today, the use of FET-based MMIC's at these frequencies has increased greatly [7]–[12]. Thus, it was planed to develop a millimeter-wave inter-satellite communications equipment, a specially developed on-board solid-state transponder. This transponder will use SSPA having an output power of 0.5 W at 38 GHz.

This paper describes the development of an MMIC amplifier module for the last stage of the SSPA. The output power of this module is 0.3 W, and was increased to 0.5 W by combining two modules using a waveguide coupler. The purpose of this paper is to make a design method of millimeter-wave high-power MMIC amplifier for satellite on-board use. For realizing this purpose, we developed a new power FET, a large signal circuit design, and high-reliable production process.

In the first part of this paper, we describe the development of a high-performance FET with a 0.25 μm long gate. To design the circuits, we needed to know FET's large-signal impedance at millimeter-wave frequencies. For this, we adopted a improved load-pull measuring method using MMIC transformers. This method and the experimental results will be discussed.

Two different MMIC's were used in the module in the final stage of the SSPA. One consisted of two FETs with 600 μm wide gates, and the other consisted of four FET's with 400 μm wide gates. This paper will describe the design and the characteristics of these MMIC's and the module using them. To aid in MMIC circuit design, we developed an accurate passive-circuit model useful up to 40 GHz. The module uses a hermetically sealed package for higher reliability and can be used at 38 GHz. The MMIC chips and modules were screened for use on board the satellite. All chips were tested at 38 GHz, and the test method and the results will be described.

II. FET Design

To develop a high-power FET for operation at 38 GHz, we developed a new FET process technology having the following features.

1. A tungsten silicide/gold (WSi/Au) gate structure, for improved reliability.
2. A mushroom-shaped gate structure, for higher frequency operation.
3. 0.25 μm-long gates, for higher frequency operation.
4. Highly doped channels, for increased power.
5. A 50-μm unit gate width, for increased gain.

Aluminium was used for the gate metal of the conventional FET's. This posses three problems. First, it is dif-

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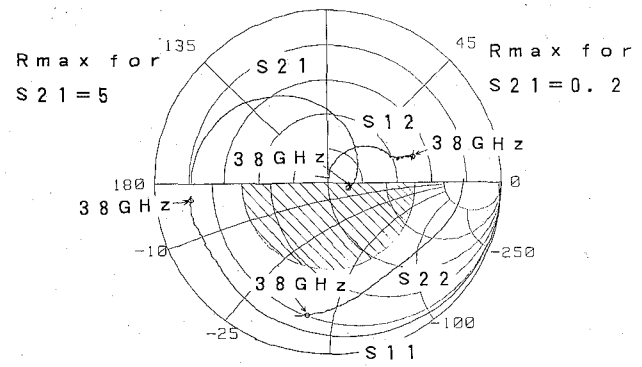

Fig. 1. S parameters of FET with 400-μm-wide, and 0.25-μm long gates. The bias canditoins are V_{ds} = 8 V, V_{gs} = 0.94 V, I ds = 57.9 mA. The frequency is from 45 MHz to 40 GHz. Small closed circles represent at 38-GHz data. The hatched area shows the tuner's coverage area viewed from the FET at 38 GHz. The area is not covered the input and output impedance of the FET.

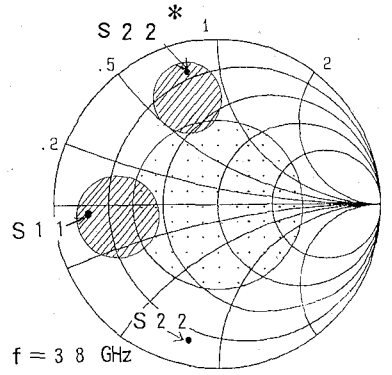

Fig. 2. Impedance coverage viewed from the FET using an external tuner. Dotted area represent for direct connection to the tuner. Closed circles represent MMIC impedance transformer use.

ficult to get a mushroom-shaped gate structure with aluminium. Second, aluminium's migration is about 10^5 A/cm^2. This reduces the reliability of a high-power FET. Third, gate resistance increases as the gate length is reduced. This degrades the high-frequency performance. To solve these problems, we used a WSi/Au gate structure and gold to achieve the mushroom-shaped gate. This increases the migration to 10^6 A/cm^2, and improves reliability because grain size of WSi is smaller than that of aluminium.

When the gate length is shortened, the thin highly-doped channel is need. Therefore, we used a thin highly-doped channel (3.5×10^{17} cm^{-3}). To determine if there are any problems associated with this channel, we also fabricated a normally-doped channel FET (1.7×10^{17} cm^{-3}) and compare the characteristics. The results of this investigation showed that the gm of the highly-doped FET is 20 mS larger, its Cgs is larger, its Ga(max) at 26.5 GHz is 1.2 dB higher, and its drain leakage current at the pinch-off voltage is lower than that of the normally-doped FET with a 600 μm wide gate. Thus, there are no problems even if a highly doped epitaxal wafer is used.

The unit gate width was investigated at this time because this FET would be used at millimeter-wave frequencies. For this purpose, we fabricated and compared the characteristics of FET's having 50- and 75-μm unit gate widths. The overall gate width of both FET's was 600-μm (50-μm $\times$ 12, or 75-μm $\times$ 8). The Ga(max) of the 50-μm unit gate width FET was 0.7 dB higher. Thus the 50-μm unit gate width was chosen.

After further study, FETs with 400-μm and 600-μm gate widths were developed for the MMICs to be used in the final stage of the SSPA. The S-parameter measurement of the FET with 400-μm gate width are shown in Fig. 1. To measure S-parameters, the FET's were secured to a metal carrier to ensure that the thermal conditions under test were the same as those in the amplifier. The Ga(max) at 38 GHz for the FET's 400-μm-wide gates was 5 dB, and 6 dB for the FET's with 600-μm-wide gates.

III. Improved Load-Pull Measurements

Large-signal impedance matching is required [13] because the MMIC is a high-power amplifier. Measurement of the large-signal impedance of a FET operating at millimeter-wave frequencies is difficult for the following reasons:

1) The large-signal impedance can be accurately measured using an RF wafer probe, and a tuner [14]. However, the tuner's coverage as viewed from the FET cannot cover the optimum input-output impedance position in the neighborhood of the FETs matching impedance S-parameter conjugate as shown in Figs. 1 and 2. This is because the impedance of $S11$ and $S22$ of the FET is low in the millimeter-wave band, and because there is a large loss between the FET and the tuner.

2) An MIC tuner near the FET prevents loss, but the bonding wires between the tuner and FET vary in length, making accurate measurement difficult.

To solve these problems, we used an MMIC impedance transformer to convert the tuner's coverage area to that shown by the hatched area in Fig. 2. This area includes the conjugate matching impedance of the FET. The measuring system shown in Fig. 3. can measure the large-signal impedance accurately because it uses no bonding wires and uses a wafer probe to measure impedance. The MIC transformer converts the tuner coverage to a small area as viewed from the FET even if the tuner's reproducibility is somewhat low. This greatly improves measurement accuracy. To calculate the impedance as viewed from the FET, the MMIC matching circuit must be evaluated accurately. Therefore, we measured the matching circuit separately.

A few problems remain to be solved. First, when the tuner is operated, vibration is transmitted to the MMIC through the probe, shifting the contact point of the probe. This problem was solved by separating the probe from the MMIC when the tuner is operated. The MMIC transformer keeps the reproducibility error due to re-contact below 1° as viewed from the FET, so no measurement problem is raised. Second, there is loss between the MMIC transformer and the tuner, so the output power

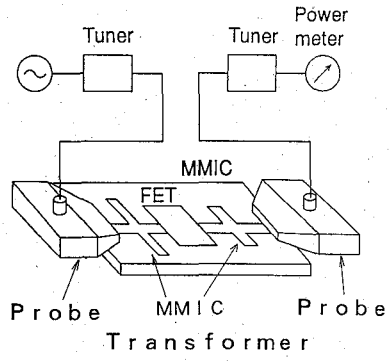

Fig. 3. Impedance measurement system using an MMIC impedance transformer.

rapidly drops as the tuner's impedance goes into the high VSWR region. Therefore, we didn't use the tuner in the high VSWR region. For this reason, we can research only a small hatched area as shown in Fig. 2. Even so, this impedance conversion method can realize a high impedance as viewed from the FET. And no problem arise because the optimum large-signal impedance is in the neighborhood of conjugate impedance of the FET *S*-parameter.

We designed and produced two types of FET, one with 400-μm-wide gates, and the other with 600-μm-wide gates. Each FET with MMIC transformer has a maximum gain at a frequency of about 33 GHz, indicating that the FET's and transformers were designed properly.

Fig. 4 shows the results of measurement of the FET's with 400-μm-wide gates. The maximum output power was 10.8 dBm and the gain was 6.1 dB when the input power was 4.7 dBm. The maximum output power and the gain were also obtained 16.2 dBm and 6.2 dB when the input power was 10 dBm, and 17.35 dBm and 4.35 dB when the input power was 13 dBm, respectively. The phase angle of the optimum impedance increases with input power. These results agree with actual experience. When the input power is high, the equivalent output power circle 1 dB down from the maximum output point tends to grow, indicating how output saturation progresses. In Fig. 5 the input-output characteristics at the optimum impedance were measured at input powers of 4.7 dBm. The difference is about 0.5 dB at saturation.

Fig. 6 shows the results of measurement of the FET's with 600 μm wide gates. The phase angle of the optimum impedance increases with increased input power, as with the FET with 400 μm wide gates. This result agrees with the optimum impedance position [11] measured using the equivalent load-pull method. The input-output characteristics at the optimum impedances were measured at input powers of 6 dBm and 16 dBm as shown in Fig. 7. The characteristic of the input power 6 dBm is considered small signal matching, and that of the input power 16 dBm is considered large signal matching. Thus, the results show that small signal matching case has higher gain when the input power below 11 dBm, and large signal matching case has higher gain when input power exceed 11 dBm.

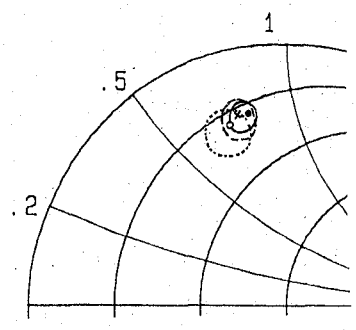

Fig. 4. Equal-power loci for a FET with 400-μm-wide gate measured at 38 GHz. The closed circle, cross, and triangle shows the maximum output power impedance, when an input powers are 4.7 dBm, 10 dBm, and 13 dBm, respectively. The output powers are 10.8 dBm, 16.2 dBm, 17.35 dBm, respectively. The solid line, broken line, dotted line circles represent the equvalent output power circule 1 dB down from each maximum output power.

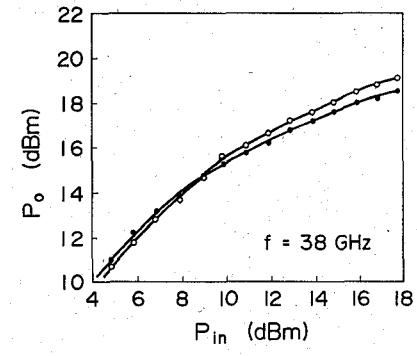

Fig. 5. Input and output power characteristics of a FET with 400-μm-wide gate. The closed circles characteristics are obtained when the output matching circuit impedance is adjusted to obtain the maximum output power at an input power of 4.7 dBm (the closed circle impedance position in the Fig. 4). The open circles characteristics are obtained when the output impedance is adjusted to obtain the maximum output power at an input power of 10 dBm (triangle impedance position in Fig. 4).

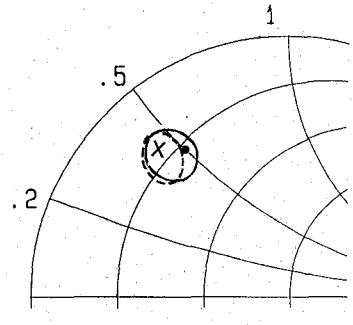

Fig. 6. Equal-power loci for a FET with 600-μm-wide gate, measured at 38 GHz. The closed circle, and cross shows the maximum output power impedance, when an input powers are 6 dBm, and 16 dBm, respectively. The output powers are 9.3 dBm, and 20.1 dBm, respectively. The solid line, broken line circles represent the equvalent output power circle 1 dB down from each maximum output power.

The difference between the characteristics was 1.5 dB when the input power was 17.5 dBm. Other chip was mounted on a metal carrier, and MIC circuit was connected outside the chip, then the circuit was adjusted so that the maximum output was obtained at 16 dBm input power. The input-output characteristics of the chip agreed

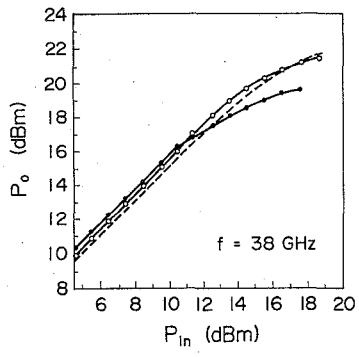

Fig. 7. Input and output power characteristics of a FET with 600-μm-wide gate. The closed circles characteristics are obtained when the output matching circuit impedance is adjusted to obtain the maximum output power at an input power of 6 dBm (the closed circle impedance position in the Fig. 6). The open circles characteristics are obtained when the output impedance is adjusted to obtain the maximum output power at an input power of 16 dBm (cross impedance position in the Fig. 6). The broken line shows the characteristics of a chip using an MIC tuner to obtain the highest power when the input power is 16 dBm.

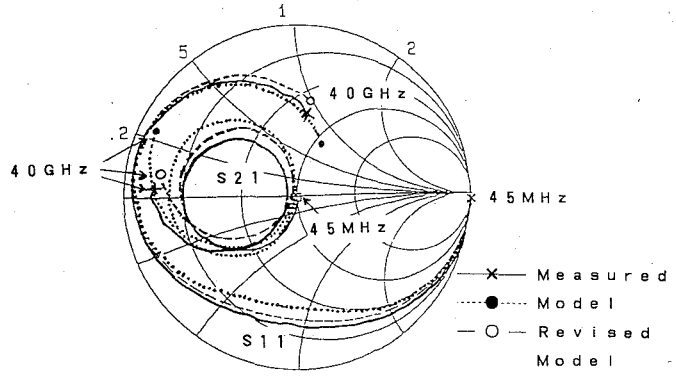

Fig. 8. Impedance loci of a matching circuit, measured from 45 MHz to 40 GHz. The solid, dotted line, and broken line are the measured data, data from the equivalent circuit model using Touchstone version 1.7, and data from the modified equivalent circuit model, respectively.

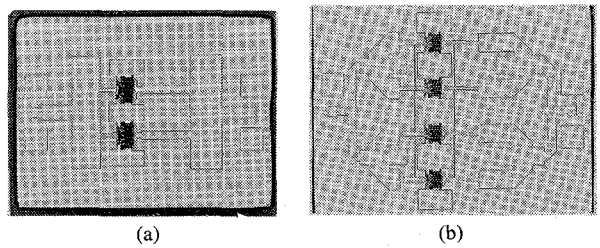

Fig. 9. (a) Photographs of the FLR056XV/ETS chip, which is composed of two FET cells with 600 μm wides gates. The chip measures 1.35 $\times$ 1.8 mm. (b) Photographs of the FLR066XV/ETS chip, which is composed of four FET cells with 400 μm wides gates. The chip measures 1.55 $\times$ 1.95 mm.

with the data using this method as shown in Fig. 7. This shows that this measurement method is reliable.

IV. MMIC Amplifier Design

The two-stage amplifier consists of two different MMICs: the names are FLR056XV/ETS and FLR066XV/ETS. FLR056XV/ETS consists of two FET's with 600-μm-wide gates, and FLR066XV/ETS consists of four FETs with 400-μm-wide gates. FLR056XV/ETS is used in the driver stage, and FLR066XV/ETS is used in the last stage.

The in-phase combiner circuits was used for reducing the chip size. Large-signal circuit design using in-phase combiners was a problem. When we design a amplifier without in-phase combiner, the optimum impedance viewed from the FET is easily realized. Because the output impedance viewed from the FET can be known by calculating the passive output matching circuit. In a combined circuit, however, the impedance viewed from the FET can be obtained only when the other FET is operating. If an attempt is made to measure the impedance of a terminal by removing one FET, the balance of the combined circuit is lost and the impedance cannot be measured correctly. In an in-phase combined circuit, connecting the ports operating in parallel with a zero-length line does not affect operation. Therefore, the output circuit terminals connecting with the FET's were stlaped by a zero-length line, and we calculated the impedance of the output circuits. But the characteristic impedance viewed from the FET terminals was 12.5 Ω for the four FETs combiner case. The impedance was converted to 50 Ω system by connecting an ideal transformer. The impedance viewed from here is equal to that viewed from one FET operating in parallel. We used this ideal transformer when the circuit was designed.

Circuit calculations were based on Touchstone program version 1.7. This passive circuit model is guaranteed for frequencies up to 20 GHz. Furthermore, our circuit is fabricated on a GaAs substrate. Therefore, the programs passive circuit model was modified and used. The circuit is a combined circuit consisting of multiple FET's. Therefore, each input and output passive circuit was looped at the FET and a single test terminal provided for each circuit. Three different line length patterns were fabricated to the correct the passive model. In the passive circuit of the FLR056XV/ETS, the effective line width 5% to 10% thinner than the actual pattern. In the case of the FLR066XV/ETS pattern, we found that, 120- and 140-μm-wide lines are 40% thinner than the actual pattern. Fig. 8 shows an example.

For the FLR066XV/ETS, oscillation was prevented by inserting an oscillation prevention circuit in the neighborhood of the FET, as shown in Fig. 9(b). This circuit consist of the thine line by straping the ports operating in parallel. For RF inspection of all chips, co-planar lines were used for input and output.

V. MMIC Performance

Fig. 9 shows the fabricated chips. The FLR056XV/ETS measures 1.35 $\times$ 1.85 mm and FLR066XV/ETS 1.55 $\times$ 1.95 mm. As described in the preceding section, these MMICs can be measured with an RF wafer probe. Fig. 10 shows the typical gain characteristics of a FLR066XV/ETS mounted on the metal carrier. The characteristics agree with the calculations.

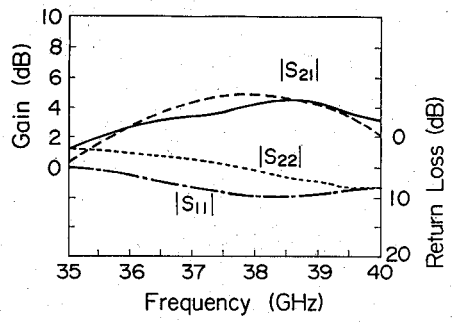

Fig. 10. Typical frequency characteristics of the FLR066XV/ETS on a metal carrier. The broken line represents the predicted characteristics. Other lines are data measured using an RF wafer probe.

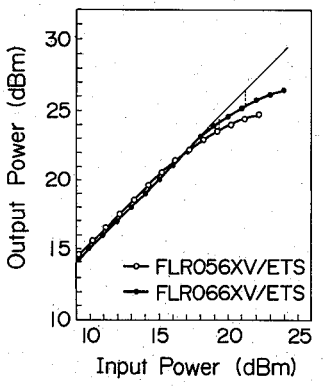

Fig. 11. Input and output characteristics of the FLR056XV/ETS and FLR066XV/ETS measured using a test fixture.

The chip was secured to a metal carrier and its characteristics measured (Fig. 11). The gain, Po (1 dB), and efficiency of the FLR056XV/ETS were 5.4 dB, 23.5 dBm, and 12%, and 5.1 dB, 25.2 dBm, and 11% for the FLR066XV/ETS. The temperature characteristic from −10°C to 50°C was 0.028 dB/°C for the FLR056XV/ETS and 0.023 dB/°C for the FLR066XV/ETS.

VI. Amplifier Module Design and Performance

A module consisting of two stages (first stage: FLR056XV/ETS, second stage: FLR066XV/ETS) sealed in a package was designed and fabricated. Sealing was used control module reliability and to improve the module's environmental resistance. The module was to operate at a high frequency (38 GHz), so a 3 × 10 × 1 mm cavity was selected. The package can prevent wave-guide-mode resonances up to 45 GHz. The RF terminals consist of sealed micro-strip lines, and the transmitting loss of a terminal is 0.2 dB. Four dc terminals extend vertically downward and a low-pass filter to cut off the RF signal is incorporated into the terminal passage. The package base is copper, so the thermal resistance is low, but the thermal expansion rate is two times that of GaAs. Therefore, a chip base made of a copper-tungsten alloy was inserted under the MMIC to reduce stress during die bonding. A dc blocking and a bias circuit were provided between boards connecting the MMIC's.

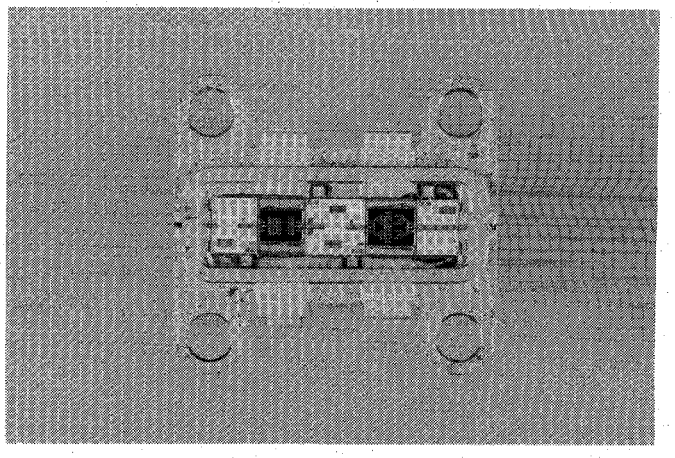

Fig. 12. Photograph of the module.

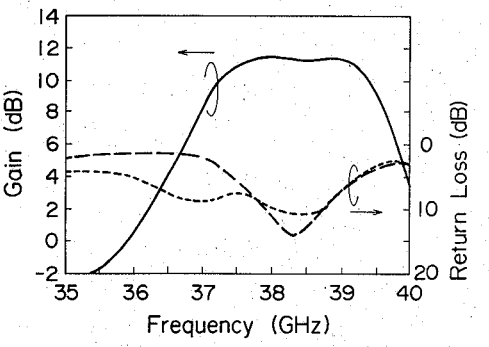

Fig. 13. Typical module frequency characteristics.

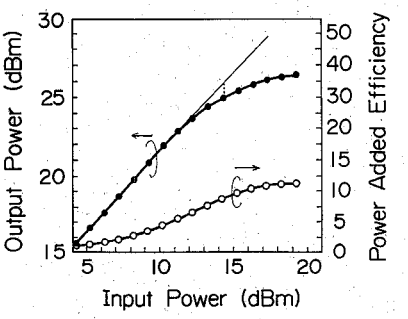

Fig. 14. Typical module input and output characteristics.

Figs. 12 to 14 show the fabricated module. A gain exceeding 11 dB was obtained over a wide band (1.5 GHz) from 37.5 GHz to 39.0 GHz at room temperature. Po (1 dB) and Po (sat) were 25.0 dBm and 26.5 dBm. The power-added efficiency was 12%, and the temperature characteristic of the module was 0.074 dB/°C from −10°C to 50°C.

VII. Amplifier Module Screening for Quality Assurance

Developed as a module to be used aboard the ETS-VI satellite, the amplifier module was manufactured in processes grounded on reliability assurance. This is the first millimeter-wave-band MMIC to be used in the satellite.

In this screening process, we adopted RF probe test to the MMIC chip. This is the first RF probe test in millimeter-wave frequencies. Namely, after dc and wafer pilot tests, the gain characteristics of all chips to be shipped are checked at 38 GHz. Because the characteristic in the 38-GHz band cannot be presumed from the DC characteristics. This process can ensure the final characteristics of the assembled modules. Mounting a chip in a package changes the thermal condition of the chip and the bonding wire effects of the RF characteristic. Therefore, the specification for screening test in chip measurement was established by measuring how the characteristics of a chip are affected by mounting it. Fig. 15 shows how the FLR066XV/ETS characteristics change. From this data, the specification of RF probe test was determined. Of 242 FLR056XV/ETS devices tested, 190 were acceptable, the average gain was 4.87 dB, and the variation in gain was 0.27 dB. Of 218 FLR066XV/ETS devices tested, 153 were acceptable, the average gain was 3.18 dB, and the variation in gain was 0.21 dB. The RF inspection reduces RF characteristic variation, thus increasing the yield in subsequent assembly tests.

Following screening tests were also done, temperature cycling (−55 to 125°C, 30 min., 25 cycle), Mechanical shock test (1500 G, 0.5 mS, Y1, once), Constant acceleration (5000 G, Y1, 1 min, once), PIND (60 Hz, 20 G), dc burn-in (Tj = 90%, 168H), and so on.

The average pinch-off voltage was 2.6 V, and the variation was about 100 mV. The average bond pull strength of the MMIC's was a 3.83 g (specification: 2.5 g). The yield is estimated to be 87.3%. The average die shear strength was 3939 g. The probability that this strength will exceed the specification (1680 g) is 98.5%.

In the module assembly test, internal circuits were not adjusted because such a process generates fine dust such as scrap metal which may lower the yield in the PIND test. In the RF test of the modules, measuring jigs were kept in good condition, and it was confirmed before and after the test that the return loss was at least 15 dB. The gate current Ig(RF) was measured with saturated output, and the life of the MMIC was estimated from the Ig. The bias of the amplifier was designed so that Ig(RF) is small when the module is mounted. The limiter resistance to the gate current was inserted to the bias circuit.

Modules were burned-in twice to observe the change in DC characteristics and to locate problems. The RF characteristic was not checked in the intermediate test, because inserting the module into a jig causes the linear gain to change slightly (about 0.5 dB), and it is difficult to check whether the RF characteristic truly changed.

Fig. 16 shows an example of module characteristics in the final test of 49 modules. The gain was 10.5 dB to 12.5 dB. The output level was 23.5 dB to 25 dB. As mentioned earlier, the gain and output level changed little even though modules were not adjusted. This indicates that the RF inspection of the chips was effective.

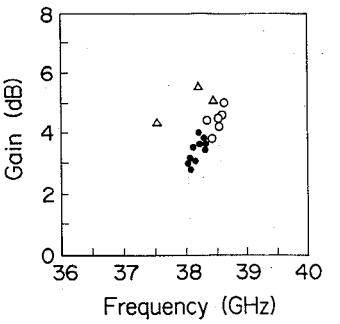

Fig. 15. Gain and peak frequency characteristics of the FLR066XV/ETS. The solid circles represent bare chip measurement using RF wafer probe. The open circles represent measurement using an RF wafer probe with the chip mounted on a metal carrier. The open triangles represent measured by using a test fixture.

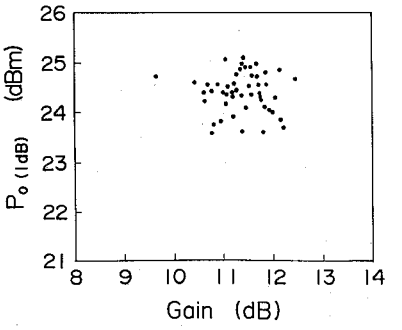

Fig. 16. Module gain and output power measured at 1-dB gain compression at final electrical test.

Three modules were selected for use in the SSPA's to be used on board the ETS-VI. Others were kept as spares, for testing, for confirming reliability, and for checking module reliability. The failure rate of the modules to be used is given by

$$\lambda_P = [\Sigma N_C \lambda_C \Pi_C + (N_R \lambda_R + \Sigma N_1 \lambda_1 + \lambda_S) \cdot \Pi_F \Pi_E] \Pi_Q \Pi_D \quad (1)$$

where λ_P: failure rate (10^{-6}/hour), Nc: stress coefficient, λ_C: failure rate of the MMIC, Π_C: acceleration coefficient, N_R: number of film resistors, λ_R: failure rate of film resistor, N_1: number of connection points, λ_1: Failure rate of the interconnection, λ_S: failure rate of the package, Π_F: environment coefficient, Π_Q: quality efficiency, and Π_D: mounting density. If the temperature changes from −25°C to 85°C, λ_P is estimated to be 0.2888 × 10^{-6}/hour (288.8 FIT) or less. Now, temperature accelerated test is done for estimating module life.

VIII. Conclusion

We have developed MMIC amplifier modules to be used in the 38-GHz SSPA for a millimeter-wave inter-satellite communications device to be carried on board the ETS-VI satellite. FET's with 0.25-μm-long gates and a highly doped epitaxial layer (carrier density: 3.5 × 10^{17} cm^{-3})

were developed for use in these MMIC's. A WSi/Au gate metal structure was used for high reliability. The large signal impedance of the FET at 38 GHz was measured with an improved load-pull method using an MMIC transformer. This method converts tuner impedance coverage as viewed from the FET to the neighborhood of the conjugate impedance of the FET *S*-parameter. Impedance conversion reduces the variations in the FET. This method was used to measure the large-signal impedance of FETs with 600-μm and 400-μm-wide gates. The passive circuit was measured at frequencies up to 40 GHz and a highly precise passive circuit was produced by modifying the 20-GHz Touchstone circuit model. As a result the obtained characteristics were almost as designed. The gain and Po (1 dB) of four combined FET's were 4.5 dB and 25.1 dBm. A strip line interface package that can be used at 38 GHz was developed, and the two-stage MMIC amplifier sealed in it. The gain and Po (1 dB) of the amplifier were 11 dB and 25 dBm. Screening of chips to be used on board the satellite was done to ensure reliability. RF inspection of the MMIC chips increased the yield in mass production.

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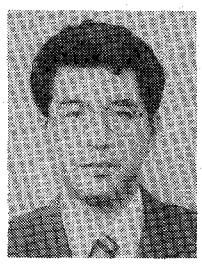

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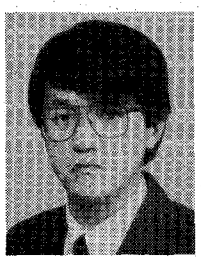

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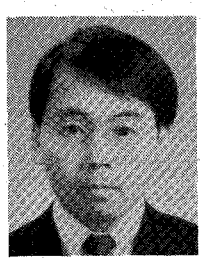

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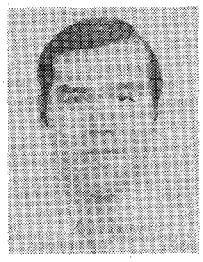

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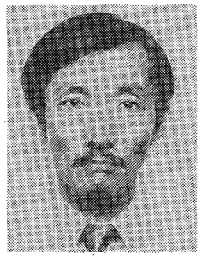

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